

REMARKS

Claims 1 to 20 are pending in the present application. Claims 15-20 have been allowed. Claims 1-14 have been rejected. Accordingly, claim 1 is herewith amended to assist in overcoming the rejection. The disclosure is also objected to. Accordingly, the disclosure is herewith amended to overcome the objection. The amendments add no new matter.

The examiner rejected claims 1 to 6 and 9 to 12 under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art in Figure 2. Applicants respectfully traverse this rejection.

A reference must teach or suggest all elements of a claim to anticipate the claim. In the amended claim 1, submitted herewith, applicants disclose and claim a read/write amplifier for a DRAM memory cell comprising, *inter alia*, a plurality of bit lines 12 and a plurality of reference bit lines 13. (Figure 3). Furthermore, the application, as amended, discloses and claims that the first read/write amplifier element 40 is located at a first end of the bit line pairs 16, and the second read/write amplifier element 50 is located at a second end of the bit line pairs 16. (Figure 3). Finally, the amended claim 1 clarifies that "the bit line pairs are activated or can be activated with the read/write amplifier. (page 12), lines 1-4; 21-30). Thus, Figure 2 of the application does not teach or suggest all elements of amended claim 1.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-6 and 10-12 under 35 U.S.C. 102(a) as anticipated by applicant's admitted prior art in Figure 2.

The Examiner rejected claims 1-14 under 35 U.S.C. 103(a) as being obvious in view of U.S. Patent No. 4,367,540 to Shimohigashi. Applicants respectfully traverse this rejection.

A reference or a combination of references must teach or suggest all elements of a claim to render the claim obvious. Shimohigashi does not teach or suggest all elements of the current invention as claimed. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims

Shimohigashi discloses a dynamic memory with an interchangeable pair of data lines and sense amplifiers, wherein a first pair of the data lines is connected to one differential sense amplifier and a second pair of the data lines is connected to another differential sense amplifier. Therefore, under Shimohigashi, a plurality of sense amplifiers are needed, in

particular, the same number of sense amplifiers is needed as data line pairs are provided in the dynamic memory.

In contrast, the inventive device discloses and claims amplifier components divided between the two provided read/write amplifier elements, and the provided bit line pairs are activated or can be activated by a single read/write amplifier.

As disclosed, the space requirement for the read/write amplifier circuits in the entire DRAM memory according to the invention can be considerably reduced compared with Shimohigashi, since a plurality of bit line pairs may now be evaluated by one and the same read/write amplifier which has merely been divided between two amplifier elements.

Thus, the invention makes it possible to produce an area-optimized DRAM read/write amplifier circuit which has only a small space requirement and with which the evaluation of DRAM memory cells, in particular of memory cells with a single memory cell array, can be evaluated with high reliability and speed.

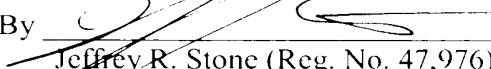
Thus, Shimohigashi fails to teach or suggest all elements of the claimed invention.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-14 as being obvious in view of U.S. Patent No. 4,367,540 to Shimohigashi

In view of Applicant's amendments and remarks, the specifications and claims are believed to be in condition for allowance. Reconsideration, withdrawal of the rejections, and passage of the case to issue is respectfully requested. If any fees not accounted for above are due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 02-3732.

Respectfully submitted,

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